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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,193	PIERCE, JOHN L.	
	Examin r	Art Unit	
	David E Graybill	2827	

-- Th MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *8-11,13-16,20 and 23-40* is/are pending in the application.

4a) Of the above claim(s) *36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-11,13-16,20,23-35 and 37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Newly submitted claim 36 is directed to an invention that is independent or distinct from the elected invention for the following reasons: it is drawn to the non-elected species. Accordingly, claim 36 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

The declaration filed on 3-18-4 under 37 CFR 1.131 has been considered but is ineffective to overcome the Hirashima reference.

The evidence submitted is insufficient to establish a reduction to practice of the invention in this country or a NAFTA or WTO member country prior to the effective date of the Hirashima reference. Specifically, the declaration does not explicitly allege a reduction to practice of the invention prior to the effective date of the Hirashima reference, and the evidence does not show that applicant performed a process that met every element of the claimed process.

The evidence submitted is insufficient to establish a conception of the invention of claims 23, 24, 27-31 and 37-40 prior to the effective date of the Hirashima reference. While conception is the mental part of the inventive act, it must be capable of proof, such as by demonstrative evidence or by a complete disclosure to another. Conception is more than a vague idea of how to solve a problem. The requisite means themselves and their interaction must also be comprehended. See *Mergenthaler v. Scudder*, 1897

C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897). In particular, there is no evidence of conception of the invention of claims 23, 24, 27, 28, 30, 31 and 36-40.

However, the declaration is sufficient to establish conception of the invention of claims 8-11, 13-16, 20 and 32-35.

The evidence submitted is insufficient to establish diligence from a date prior to the date of reduction to practice of the Hirashima reference to either a constructive reduction to practice or an actual reduction to practice. Specifically, applicant has merely alleged that applicant had been diligent but has shown no evidence of facts establishing diligence. See MPEP 715.07(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 9, 32-34 and 37, 38 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hirashima (6400019) and Blumberg (6387830).

At column 3, line 60 to column 6, line 46, and column 8, line 19 to column 11, line 24, Hirashima teaches the following:

A method of producing a wafer-interposer comprising the steps of: attaching one or more first electrical contacts 7a to a lower surface of a substrate 1Bi comprising a material; attaching one or more second electrical contacts 7b to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts; and creating one or more first electrical pathways 10 passing through the substrate and connecting the first electrical contacts to the second electrical contacts; wherein the first and second electrical contacts are connection pads; mounting the substrate on a semiconductor wafer including at least one semiconductor die 1CS; wherein the step of mounting the substrate on the semiconductor wafer further comprises the step of depositing a conductor 1BA on at least one third electrical contact 6BP on an upper surface of the semiconductor wafer, the at least one third electrical contact being associated with the at least one semiconductor die; aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the at least one third electrical contact correspond with the first electrical contacts on the lower surface of the substrate; mounting the substrate on a least one semiconductor wafer including at least one semiconductor die; attaching the substrate and semiconductor wafer assembly to a testing apparatus; and testing a portion of the at least one semiconductor die; wherein the step of testing the portion of the at least one

semiconductor die further comprises performing parametric testing on at least one of the dies; grading one or mote performance characteristics of each semiconductor die during testing.

To further clarify the teaching of attaching the substrate and semiconductor wafer assembly to a testing apparatus; and testing a portion of the at least one semiconductor die, performing parametric testing on at least one of the dies, the step of grading one or more performance characteristics of each semiconductor die during testing, it is noted that at column 6, lines 7-13, Hirashima teaches a "bending test." Moreover, it is inherent that parametric testing is performed in the bending test because a bending parameter is tested. In addition, it is inherent that the substrate and wafer assembly is attached to a testing apparatus during testing; at least, because the substrate and wafer assembly are attached to the "mobile telephone" and "push buttons" during a bending test. Also, a step of grading is inherent in the process of testing because it is inherent that the purpose of the testing is for sorting the dies.

However, Hirashima does not appear to explicitly teach the substrate comprising a B-Stage adhesive material.

Nonetheless, at column 2, lines 41-49; column 4, lines 277; and column 5, lines 24-56, Blumberg teaches a substrate 100 comprising a B-Stage adhesive material. Furthermore, it would have been obvious to

combine the process of Blumberg with the process of Hirashima because it would facilitate provision of the substrate of Hirashima.

Claims 10, 11, 13, 14-16, 20, 23, 24, 28-30 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirashima and Blumberg as applied to claims 8, 9 and 32, and further in combination with Tsai (6489180).

As cited, Hirashima teaches the following:

A method for producing a wafer-interposer assembly comprising the steps of: attaching one or more first electrical contacts to a lower surface of a substrate, the substrate comprising a material; attaching one or more second electrical contacts to an upper surface of the substrate, the second electrical contacts having greater surface area and greater pitch than the first electrical contacts; creating one or more first electrical pathways passing through the substrate and connecting the first electrical contacts to the second electrical contacts; depositing a conductor 1BA on one or more third electrical contacts 6BP on an upper surface of a semiconductor wafer 1CS, the semiconductor wafer including one or more semiconductor dies 1CS and the third electrical contacts being associated with the semiconductor dies; aligning the substrate with the semiconductor wafer so that the deposits of the conductor on the third electrical contacts correspond with the first electrical contacts on the lower surface of the substrate; attaching the

substrate to the semiconductor wafer; wherein the first, second and third electrical contacts are connection pads, applying additional metallization 3, 6 to one or more of the third electrical contacts to redistribute them prior to the attachment of the substrate, adding additional metallization 3 to one or more of the third electrical contacts to improve the contact between the conductor and the third electrical contacts; wherein the step of attaching the substrate to the semiconductor wafer comprises the steps of: placing the semiconductor wafer on a first flat surface 1Bi and holding the semiconductor in place (via underfill 1UF); placing the substrate on a second flat surface 1CS and holding the substrate in place (via underfill); and bringing the first and second flat surfaces together so that the semiconductor wafer and the substrate form an adhesive bond (via underfill); wherein each conductor is a solder ball, attaching the substrate and semiconductor wafer assembly to a testing apparatus; and testing at least one of the semiconductor dies; wherein the step of testing the semiconductor dies further comprises performing parametric testing on at least one of the dies, the step of grading one or more performance characteristics of each semiconductor die during testing, singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies, and the step of sorting the semiconductor die assemblies based on the one or more performance characteristics; wherein

the step of mounting the substrate on the semiconductor wafer further comprises the step of applying a layer of underfill 1UF to the upper surface of the semiconductor wafer.

To further clarify the teaching of attaching the substrate and semiconductor wafer assembly to a testing apparatus, and testing at least one of the semiconductor dies, performing parametric testing on at least one of the dies, the step of grading one or more performance characteristics of each semiconductor die during testing, and the step of sorting the semiconductor die assemblies based on the one or more performance characteristics, it is noted that at column 6, lines 7-13, Hirashima teaches a "bending test." Moreover, it is inherent that parametric testing is performed in the bending test because a bending parameter is tested. In addition, it is inherent that the substrate and wafer assembly is attached to a testing apparatus during testing; at least, because the substrate and wafer assembly are attached to the "mobile telephone" and "push buttons" during a bending test. Also, a step of grading is inherent in the process of testing because it is inherent that the purpose of the testing is for sorting the dies. Similarly, the step of sorting the semiconductor die assemblies based on the bending performance characteristics is inherent in the bending test.

To further clarify the step of singulating the substrate and semiconductor wafer assembly into one or more semiconductor die

assemblies, the substrate and wafer assembly are singular; therefore, it is inherent that they are singulated.

In addition, as applied supra, Blumberg teaches the B-Stage adhesive material.

Although as cited, Hirashima teaches applying a layer of underfill 1UF to the upper surface of the semiconductor wafer, Hirashima does not appear to explicitly teach that the underfill is "no-flow."

Regardless, at column 2, lines 5-8, Tsai teaches no-flow underfill 130. Moreover, it would have been obvious to use the no-flow underfill as the underfill of Hirashima because it would provide the underfill of Hirashima and help prevent short-circuits.

Claims 16, 23, 24 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirashima, Blumberg and Tsai as applied to claims 10, 11, 13, 14 and 20, and further in combination with Kline (6483043).

Hirashima does not appear to explicitly teach attaching the substrate and semiconductor wafer assembly to a testing apparatus, and testing at least one of the semiconductor dies; wherein the step of testing the semiconductor dies further comprises performing parametric testing on at least one of the dies; wherein the step of testing the semiconductor dies further comprises testing the semiconductor dies simultaneously, the step of grading one or more performance characteristics of each semiconductor die

during testing, singulating the substrate and semiconductor wafer assembly into one or more semiconductor die assemblies, the step of sorting the semiconductor die assemblies based on the one or more performance characteristics, and sorting the semiconductor die assemblies into conforming and nonconforming groups.

Notwithstanding, at column 6, lines 21-45, Kline teaches this process. Furthermore, it would have been obvious to combine the process of Kline with the process of the applied prior art because it would enable testing.

Claims 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Hirashima and Blumberg as applied to claim 8 supra, and further in combination with Kline (6483043).

The combination of Hirashima and Blumberg does not appear to explicitly disclose mounting the substrate on a least one semiconductor wafer including at least one semiconductor die; attaching the substrate and semiconductor wafer assembly to a testing apparatus; and testing a portion of the at least one semiconductor die; wherein the step of testing the portion of the at least one semiconductor die further comprises performing parametric testing on at least one of the dies; wherein the step of testing the portion of the at least one semiconductor die further comprises testing the semiconductor dies simultaneously; grading one or mote performance characteristics of each semiconductor die during testing.

Nonetheless, Kline discloses this process, and is applied to the claims for the same reasons it was applied to claims 16, 23, 24 and 27-31 supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Applicant's remarks filed 3-18-4 have been fully considered and are adequately addressed by the rejections supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Head SAE Linda Hodge-Taylor whose telephone number is 571-272-1585.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
29-May-04